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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,246	11/19/2001	Shigetoshi Tomio	1450.1013	8345

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EXAMINER	
LAO, LUN YI	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,246	TOMIO ET AL.	
	Examiner	Art Unit	
	LUN-YI LAO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-13* is/are allowed.

6)☒ Claim(s) *1,7,8,14,15 and 17* is/are rejected.

7)☐ Claim(s) *2-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 17 recites the limitation of "said first and second signal line" in claim 17, line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 7-8 and 14-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Takamori et al(6,867,552)

As to claims 1, 7-8 and 14-15, Takayama et al teach a driving circuit for a flat display device(plasma display(see figures 10, 14A and column 8, lines 23-25) applying a first voltage(+Vs/2) to a first electrode(Y) of a capacitive load(100)serving as a display element and applying a second voltage(-Vs/2) having a phase opposite to the first voltage to the first electrode(Y) of the capacitive load(100)(see figures 1, 3, 5; column 9, lines 34-55 and column 10, lines 32-54) comprising: a power supply circuit(SW1'-SW5', Vs, Vs/2, C4) for generating the first voltage(Vs/2) and the second voltage(-Vs/2) to be applied to the capacitive load(100) using an externally supplied power supply(VS, Vs/2); a capacitor(C4) between the first signal lines(OUTB') and the second signal lines(OUTA') and a ramp waveform generation circuit(SW1'-SW3', C4, Vs, Vs/2) connected between a first signal line(OUTB') supplying the first voltage(Vs/2) and a capacitor(C4) so as to generate a ramp waveform to be applied to the capacitive load(100)(see figures 1, 3, 5; column 8, lines 49-68; column 9, lines 1-55 and column 10, lines 32-54)

As to claim 7, Takayama et al teach the ramp waveform to be applied to the capacitive load(100) changes from a positive potential(Vs/2) to a negative potential(-Vs/2)(see figures 1, 5 and column 9, lines 45-55).

As to claim 8, Takayama et al teach an AC-driven plasma display device(see figure 10 and column 8, lines 23-25).

As to claims 14-15, Takayama et al teach the ramp waveform changes in its voltage with time elapse(see figures 1 and 5).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable Kishi et al's admitted prior art(6,686,912) in view of Hashimoto et al(6,483250).

Kishi et al's admitted prior art teach a driving circuit for a flat display(Plasma display) device comprising a drive circuit applying a first, high potential voltage(Vs, 180V) to a first electrode of a capacitive load(20) and applying a second, low potential voltage having a second, low potential voltage(-Vy, -180V) having a phase opposite to the first voltage to the first electrode of a capacitive load(20)(see figures 4-6 and column 5, lines 20-60); a power supply circuit(44); a capacitor(C3 or C2) and a power recover circuit(33) connected a first signal line applied the first voltage(Vs) and a ground(see figures 4-5; column 4, lines 33-63 and column 5, lines 13-20).

Kishi et al's admitted prior art fail to disclose a ramp wave form generation circuit.

Hashimoto et al teach a driving circuit for a flat display device(1)(see figure 1 and column 8, lines 20-25) comprising a ramp waveform generation circuit(14a3, 14a4) for generating a ramp waveform to be applied to the capacitive load(CP)(see figures 1-4, 9;

column 12, lines 34-52; column 13, lines 1-11 and column 18, lines 40-55). It would have been obvious to have modified Kishi et al' admitted prior art as modified with the teaching of Hashimoto et al, so as to provide a gray scale display to a user.

Allowable Subject Matter

7. Claims 2-6 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 9-13 are allowable since none of cited references teach a third switching circuit connected between the ground and the other terminal of the capacitor; and a fourth switching circuit and a first resistor, connected in series between the ground and the interconnection node between the first and second switching circuits.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jin et al(7,006,057) teach a plasma display having a ramp circuit.

Iwasa et al(6,937,213) teach a plasma display having a ramp circuit.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi Lao whose telephone number is 571-272-7671. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 23, 2006
L-Y. Lao
Lun-yi Lao
Primary Examiner